Audio Codec '97
Errata Sheet

REVISION HISTORY

1.00	AC '97 Component Specification revision 1.0, released May 17, 1996
1.01	**Page 32, 6.3:** duplicate 6.3 heading moved and renamed 6.1.1 (no text changed)
	Page 34, 6.3.1, para 2, line 3: ~~the~~ each vendors...
	Page 39, 6.3.11, para 1, line 4: ~~bits~~ bits 0-7.
1.02	AC '97 Component Specification revision 1.02, posted on the Web June 1, 1996
	Cover changed (no content changed)
1.03	AC '97 Component Specification revision 1.03, updated September 22, 1996
	Page 7, 1.1, Feature List, bullet 2: Two standard packages: 48-pins ~~package, alternate~~ and 64-pins ~~package~~
	Page 11, 2., Packaging, para 2: ...48-pin package is attractive ~~a requirement~~ for migrating *baseline motherboard*...
	Page 11, 2., Packaging, para 3: The standard ~~alternate~~ 64-pin package...
	Page 15, 2.2, Table 2: 64-pin package "Reserved" pins 41-44 assigned as generic caps or multi-channel outputs
	Page 18, 3.3, Table 5, 1st entry: Vref ~~Vref1~~
	Page 18, 3.3, Table 5: added references to CAP2, CAP11-CAP13, CAP25-CAP28
	Page 19, 3.3, bullets: added references to CAP25-CAP28
	Page 29, 5.2, para 1: ...When AC '97's ~~General Purpose Register (20h),~~ Powerdown Register (26h), is...
	Page 29, 5.2, para 2: ...the write to the ~~General Purpose Register (20h)~~ Powerdown Register (26h) with PR4.
	Page 33, 6.3, Table 7: PC_BEEP Default x000h can be 0000h or 8000h (mute off or on)
	Page 33, 6.3, Table 7: Phone Volume (0Ch) and Mic Volume (0Eh) register D5 bits: were *GN5*, now X (don't care)
	Page 36, 6.3.4, PC Beep, para 2: Inserted new 2nd paragraph and reference to AC '97 FAQ for further details.
	Page 36, 6.3.4, PC Beep, para 3: Note: The PC Beep is recommended ~~required~~ to be routed to...
	Page 36, 6.3.4, PC Beep, para 4: The default value can be 0000h or 8000h...mute off or on
	Page 38, 6.3.9, 3D Control Register: linear or logarithmic implementation is acceptable (linear is shown)
	Page 41, 7., para 1: ...by the ~~General Purpose Register (index 20h)~~ Powerdown Register (26h).
	Page 41, 7., para 2: ...writes to the ~~General Purpose~~ Powerdown Register are performed...
	Page 43, 9.1., parenthesis: ($T_{ambient}$ = 25^{0}C, AVdd = DVdd = 5.0 V or 3.3V **+/- 5%;** ...
	Page 43, 9.1., NOTE: ... either 5.0V or 3.3V **(+/- 5%),** ...
	Page 43, 9.1., para 2: added 2nd paragraph and 2 tables specifying PCI 2.1 compliant 5.0 V and 3.3 V operation
	Page 46, 9.2.3., figure: shows setup and hold times for SYNC, SDATA_OUT, and SDATA_IN (at Controller)
	Page 46, 9.2.4., table: added 6nS spec for Max rise and fall times (for all entries in table)
	Page 48, 10., parenthesis: ... $T_{ambient}$ = 25^{0}C, AVdd = DVdd = 5.0 V **+/- 5%;** ... tone and 3D disabled).
	Page 48, 10., Table: Vrefout spec'd at 2.25 - 2.75 V typical
	Page 48, 10., Note 7: added clarification of Stop Band rejection
	Page 48, 10., Note 8: added clarification of Out-of-Band rejection

Note: Pages 43 and 46 have been updated to appear as below.

9. AC-link Digital DC and AC Characteristics

9.1. DC Characteristics

($T_{ambient}$ = 25^{0}C, AVdd = DVdd = 5.0V or 3.3V +/- 5%; AVss = DVss = 0V; 50pF external load)

Parameter	Symbol	Min	Typ	Max	Units
Input voltage range	V_{in}	-0.30	-	DVdd + 0.30	V
Low level input voltage	V_{il}	-	-	0.30 x Vdd	V
High level input voltage	V_{ih}	0.40 x Vdd	-	-	V
High level output voltage	V_{oh}	0.50 x Vdd	-	-	V
Low level output voltage	V_{ol}	-	-	0.20 x Vdd	V
Input Leakage Current (AC-link inputs)	-	-10	-	10	uA
Output Leakage Current (Hi-Z'd AC-link outputs)	-	-10	-	10	uA
Output buffer drive current	-	-	5	-	mA

NOTE: It is recommended that the digital portion of the AC '97 component be capable of operating at either 5.0V or 3.3V (+/- 5%), depending on which DVdd is supplied (see section 3.4 for description of Power and Ground Signal levels).

In order to specify operation of the digital portion of the AC '97 component at both 5.0 V and 3.3 V, the low and high level input and output voltages are specified as percentages of the digital supply voltage. The AC '97 Working Group believes that it is possible to deliver dual voltage parts which meet the above specification. However, the following has been added to simplify the implementation for those who do not support dual voltage (and possibly those who do), by allowing 5.0 or 3.3 V parts to match the PCI 2.1 specifications for V_{ih}, V_{il}, V_{oh}, and V_{ol}:

5.0 V Only Operation					
Parameter	Symbol	Min	Typ	Max	Units
Input voltage range	V_{in}	-0.30	-	5.30	V
Low level input voltage	V_{il}	-	-	0.8	V
High level input voltage	V_{ih}	2.0	-	-	V
High level output voltage	V_{oh}	2.4	-	-	V
Low level output voltage	V_{ol}	-	-	.55	V

3.3 V Only Operation					
Parameter	Symbol	Min	Typ	Max	Units
Input voltage range	V_{in}	-0.30	-	3.60	V
Low level input voltage	V_{il}	-	-	1.0	V
High level input voltage	V_{ih}	1.6	-	-	V
High level output voltage	V_{oh}	2.97	-	-	V
Low level output voltage	V_{ol}	-	-	0.33	V

9.2.3. Data Setup And Hold

(50pF external load)
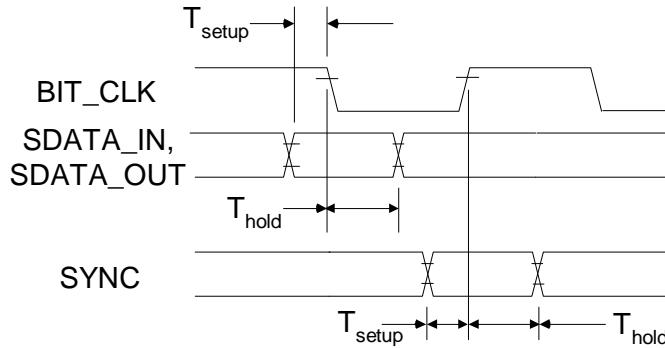
Parameter	Symbol	Min	Typ	Max	Units
Setup to falling edge of BIT_CLK	T_{setup}	15.0	-	-	nS
Hold from falling edge of BIT_CLK	T_{hold}	5.0	-	-	nS

Note 1: Setup and hold time parameters for SDATA_IN are with respect to the AC '97 Controller.

9.2.4. Signal Rise and Fall Times

(50pF external load; from 10% to 90% of Vdd)
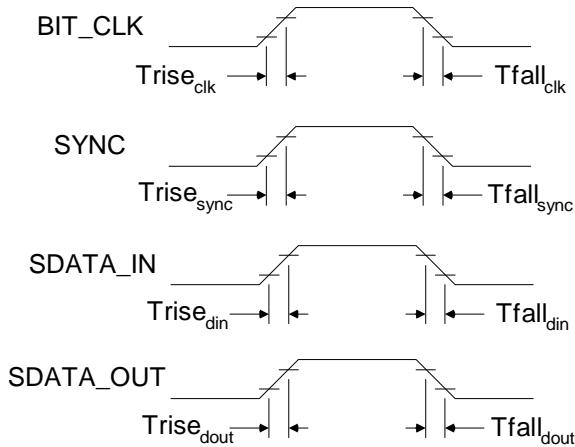
Parameter	Symbol	Min	Typ	Max	Units
BIT_CLK rise time	$Trise_{clk}$	2	-	6	nS
BIT_CLK fall time	$Tfall_{clk}$	2	-	6	nS
SYNC rise time	$Trise_{sync}$	2	-	6	nS
SYNC fall time	$Tfall_{sync}$	2	-	6	nS
SDATA_IN rise time	$Trise_{din}$	2	-	6	nS
SDATA_IN fall time	$Tfall_{din}$	2	-	6	nS
SDATA_OUT rise time	$Trise_{dout}$	2	-	6	nS