## AMD

## Flash Memory

## $\searrow$ <br> $\pm+$



Quick Reference Guide

## SPANSIO N ${ }^{w}$

## Part Number Construction

Spansion" Ordering Part Number Construction: Single-die Products


## Speed Option

Asynchronous (no CLK input)
"Speed Option" represents random access time (ns).
If greater than 100 ns , use the two leftmost digits.
Synchronous (CLK input)
"Speed Option" represents clock frequency (MHz). First digit represents 100 s of MHz . Second digit represents the speed between 0 and 99 MHz :

| A | $0-4$ | F | $25-29$ | L | $50-54$ | R | $75-79$ |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- |
| B | $5-9$ | G | $30-34$ | M | $55-59$ | S | $80-84$ |
| C | $10-14$ | H | $35-39$ | N | $60-64$ | T | $85-89$ |
| D | $15-19$ | J | $40-44$ | P | $65-69$ | U | $90-94$ |
| E | $20-24$ | K | $45-49$ | Q | $70-74$ | W | $95-99$ |

$\begin{array}{ll}\text { A } & 0-4 \\ \text { B } & 5-9\end{array}$
10-14 H 35-39
D $15-19 \quad$ J $40-44 \quad$ P $\quad 65-69$ U $90-94$
E $\quad 20-24 \quad$ K $\quad 45-49 \quad$ Q $\quad 70-74 \quad$ W $95-99$

## Temperature Grade

$\mathrm{E}=$ Engineering Samples
$\mathrm{C}=$ Commercial $\left(0-70^{\circ} \mathrm{C}\right.$
$\mathrm{W}=$ Wireless $\left(-25-85^{\circ} \mathrm{C}\right)$
I = Industrial ( $-40-85^{\circ} \mathrm{C}$ )
$\mathrm{N}=$ Extended $\left(-40-125^{\circ} \mathrm{C}\right)$

Package Material Set (Varies by Package Type)
[BGA] A = Standard Not Lead (Pb)-Free
$[B G A] F=$ Standard Lead (Pb)-Free
[Lead Frame] A = Standard Not Lead (Pb)-Free, Copper [Lead Frame] F = Standard Lead (Pb)-Free, Copper, Sn

## Package Type [Family]

$B=B G A[B G A$
= CSOP [Lead Frame]
D = Die [Die/Wafer]
$E=$ Super CSP [BGA]
$\mathrm{F}=$ Fortified BGA [BGA]
M = SOIC/SOP [Lead Frame]
$\mathrm{N}=\mathrm{WSON}$ [Lead Frame]

Spansion"' Ordering Part Number Construction: Single-die Products

| Generic OPN |  |  |  |  |  |  |  |  |  | Ordering Options |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Prefix | Series |  | Family |  |  | Density |  |  | Tech <br> D | Sector | Speed Option |  |  |  | Package |  | Temp | Option |
| Am | 2 | 9 | B | D | S | 3 | 2 | 3 |  | T | 1 | 1 | A | (R) | W | K | I |  |
| Prefix <br> Am = <br> originally | Prod 29 = NOR <br> nsion develo | ries Erase memory <br> mory <br> AMD |  |  |  | Dens <br> Density and d indica Bus w vary by | not eets. ice d nd or ily. | tables s broadly y. zation |  | Sector Ar <br> Sector Wr <br> $\mathrm{T}=$ Top b $\mathrm{B}=$ Bottom <br> U/blank = <br> $\mathrm{H}=$ Unifor <br> highe Uniform <br> $\mathrm{L}=\underset{\text { Iowes }}{\text { Unifor }}$ | itect Pro sect boot iform secto addre secto ddres |  |  |  |  | erat <br> omm <br> dust xtend | Range ( $0^{\circ}-7$ $-40^{\circ}-85$ $-55^{\circ}-1$ | $0^{\circ} \mathrm{C}$ ) <br> ${ }^{\circ} \mathrm{C}$ ) <br> $5^{\circ} \mathrm{C}$ ) |

Device Family
$\mathrm{BDS}=1.8 \mathrm{~V}$, SRW, Burst
DS $=1.8 \mathrm{~V}$, SRW
$\mathrm{SL}=1.8 \mathrm{~V}$
$\mathrm{LV}=3 \mathrm{~V}$
$\mathrm{DL}=3 \mathrm{~V}, \mathrm{SRW}$
$\mathrm{BL}=3 \mathrm{~V}$, Burst
PL $=3 \mathrm{~V}$, Page
$\mathrm{PDL}=3 \mathrm{~V}$, SRW, Page
$\mathrm{F}=5 \mathrm{~V}$
SRW = Simultaneous Read-Write

Process Technology
B: 320 nm Floating Gate C: 320 nm Floating Gate
D: 230 nm Floating Gate
G: 170 nm Floating Gate
H: 130 nm Floating Gate
M: 230 nm MirrorBit ${ }^{\text {TM }}$

Optional Processing blank = standard $\mathrm{N}=\mathrm{ESN}$ device

## Speed Option, Voltage Regulation

### 1.8V Devices

$* *(*)=(S L, D S) 2$ or 3 digits indicate speed in ns,
$\mathrm{V}_{\mathrm{CC}}=1.8-2.2 \mathrm{~V}$
$*^{*}(*)=(\mathrm{BDS}) 2$ or 3 characters indicate clock rate asynchronous read access, handshaking type.

## $3 V$ Devices

$* *(*)=2$ or 3 digits indicate speed in ns, device is full voltage range.
${ }^{*}(*) 1=($ LV64xD/G) First two digits indicate speed in ns $\times 10$. " 1 " indicates $\mathrm{V}_{\mathrm{IO}}<\mathrm{V}_{\mathrm{cc}}$
** $=(P D L)$ First digit is speed in ns $\times 10$ Last is $\mathrm{V}_{\mathrm{IO}}$ range, $3: \mathrm{V}_{\mathrm{IO}}=3 \mathrm{~V}, 8: \mathrm{V}_{\mathrm{IO}}=1.8 \mathrm{~V}$.

## 5V Devices

*(*)0 = Ends in "0" - indicates speed in ns, $\mathrm{V}_{\text {cc }}=5.0 \mathrm{~V} \pm 10 \%(4.5-5.5 \mathrm{~V})$.
*5 = Ends in " 5 " - check table or data sheet for actual speed and voltage range.
(F400) If part number has a "0" after the temperature range, then $\mathrm{V}_{\mathrm{cc}}=4.5-5.5 \mathrm{~V}$.
" $R$ " indicates regulated voltage range

## Package Type

J $=$ Rectangular Plastic Leaded Chip Carrier (PLCC)
$\mathrm{K}=80$-pin Plastic Quad Flat Package (PQFP) (PQR080)
$\mathrm{P}=$ Plastic Dual Inline Package (PDIP)
$\mathrm{S}=44$-pin Small Outline (SO) Package (SO 044)
SK $=44$-pin Small Outline (SO) Package (SO 044)
$Z=56$ pin Shrink Small Outline Package (SSOP) (SSOO56)

## Thin Small Outline Packages (TSOP):

$\mathrm{E}=32,40$, or 48Pin Standard Pinout (TS 048) (for Am29F016/017 devices only $E=48-$ pin, $E 4=40-$ pin)
E2 $=40 / 44$-pin Type-II Standard Pinout (TS 044)
$\mathrm{F}=32,40$, or 48pin Reverse Pinout (TSR048) for Am29F016/017 devices only, F = 48-pin, F4 = 40-pin)
F2 $=40 / 44$-pin Type-II Reverse Pinout (TSR044)

## Fine-Pitch Ball Grid Array Packages,

0.8 mm ball pitch (unless otherwise noted):
0.8 mm ball pitch (unless otherwise noted)

MA $=63$-ball, $11 \times 12 \mathrm{~mm}$ body (FSA063)
MD $=63$-ball, $10.95 \times 11.95$ body (FSD063)
MD $=63$-ball, $10.95 \times 11.95$ body (FSD063)
$V A=44$-ball, $9.2 \times 8 \mathrm{~mm}$ body, 0.5 mm pitch (VDA044)
$\mathrm{VK}=80$-ball, $11.5 \times 9 \mathrm{~mm}$ body (VBB080)
$\mathrm{VM}=64$-ball, $8 \times 9 \mathrm{~mm}$ (VBD064)
$W A=48$-Ball, $6 \times 8 \mathrm{~mm}$ body (FBA048)
$\mathrm{WB}=48$-Ball, $6 \times 9 \mathrm{~mm}$ body (FBB048)
$W C=48$-Ball, $8 \times 9 \mathrm{~mm}$ body (FBCO48)
WD $=63$-Ball, $8 \times 14 \mathrm{~mm}$ body (FBD063)
WG $=40$-Ball, $8 \times 15 \mathrm{~mm}$ body (FBE040)
$\mathrm{WH}=63$-Ball, $12 \times 11 \mathrm{~mm}$ body (FBE063)
WH $=$ 63-Ball
WK $=47$-Ball, $7 \times 10 \mathrm{~mm}$ body, 0.5 mm ball pitch (FDD047)
$\mathrm{WL}=48$-Ball, $11 \times 10 \mathrm{~mm}$ body, 0.5 mm ball pitch (FDE048)
$W M=48$-Ball, $6 \times 12 \mathrm{~mm}$ body (FBD048)
$\mathrm{WM}=48$-Ball, $6 \times 12 \mathrm{~mm}$ body (FBD048)
$\mathrm{WP}=84$-Ball, $11 \times 12 \mathrm{~mm}$ body (FBF084)
$\mathrm{WS}=80$-Ball, $11 \times 12 \mathrm{~mm}$ body (FBE080)

## Fortified Ball Grid Array Packages,

1.0 mm ball pitch (unless otherwise noted):

PA $=64$-Ball, $13 \times 11 \mathrm{~mm}$ body (LSA064)
$\mathrm{PB}=80$-Ball, $13 \times 11 \mathrm{~mm}$ body (LAA080)
$\mathrm{PC}=64$-Ball $13 \times 11 \mathrm{~mm}$ body (LAA064)
$\mathrm{PE}=80$-Ball, $10 \times 15 \mathrm{~mm}$ body (LAB080)
PG $=64$-Ball, $18 \times 12 \mathrm{~mm}$ body (LAC064)
$\mathrm{PH}=80$-Ball, $13 \times 11 \mathrm{~mm}$ body (LSB080)
$\mathrm{PI}=80$-Ball, $11 \times 12 \mathrm{~mm}$ body (LSC080)

## Spansion"' Ordering Part Number Construction: Single-die Products (230nm, 330nm technology)


(MBM)
Spansion"' Ordering Part Number Construction: Single-die Products (I70nm technology and newer)


MBM $=$ Spansion $^{\text {TM }}$ memory originally developed by Fujitsu

Dual. dual operation
$A=$ Conventional
B $=$ Burst, Dual
no handshake
$D=$ Dual
$F=$ Burst, Dual,
handshake
$P=$ Page
$\mathrm{Q}=$ Page, Dual
R = Page, Dual,Multi CS
$X=$ Page, Dual, x32

## Density, $1 / 0$

$32=32 \mathrm{Mb}, \times 8 / \times 16$ Flexible Bank
$34=32 \mathrm{Mb}, \times 8 / \times 16$ Sliding Bank
$64=64 \mathrm{Mb}, x 8 / \times 16$
$65=64 \mathrm{Mb}, \times 16$
$96=96 \mathrm{Mb}, \times 16$
$12=128 \mathrm{Mb}, \times 8 / \times 16$, x16/x32

Note: Please contact your local sales office for information on any OPN's that are not covered by the above structures.

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