**MirrorBit Flash Array Layout**

metal lines

**MirrorBit Cell**

word lines

gate

storage element

bit lines

storage elements

contact to source/drain

source/drain

source/drain

silicon

*Figure 1: MirrorBit™ technology's symmetric design doubles the density of a Flash memory array. In addition, the MirrorBit array layout greatly simplifies the manufacturing process.*



**Intrinsic Yield Comparison**

MLC Floating Gate

MirrorBit™ Technology

Yield loss

**Yield enhancement**
Fewer critical mask steps

**Yield enhancement**
Better word line spacing

Number **=Z**
of Good
Die (MLC)

Number of **=130% x Z**
Good Die
(MirrorBit
technology)

Higher manufacturing yield translates into a better cost structure. MirrorBit technology's simple memory array layout results in intrinsic yields as much as 30% higher than MLC floating gate technology.
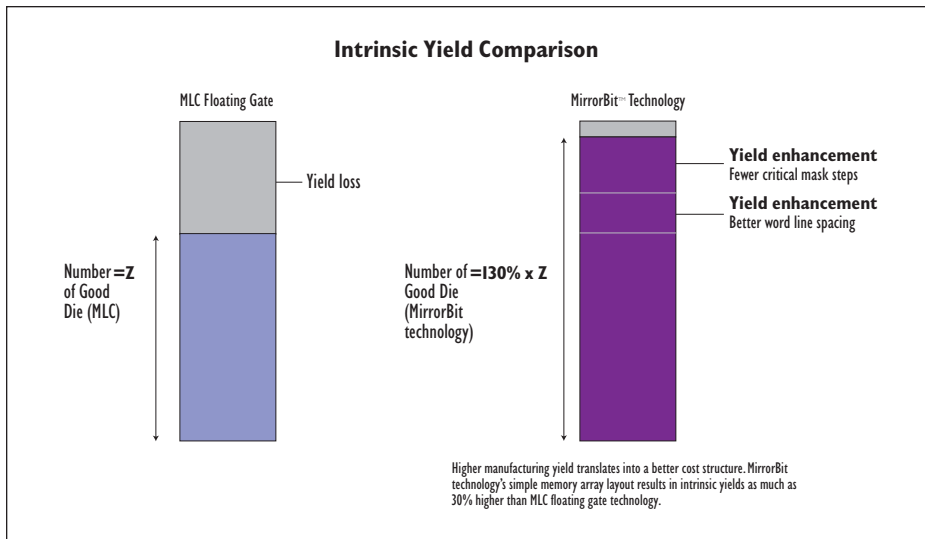
*Figure 2: MirrorBit™ technology results in an industry-leading cost structure.*