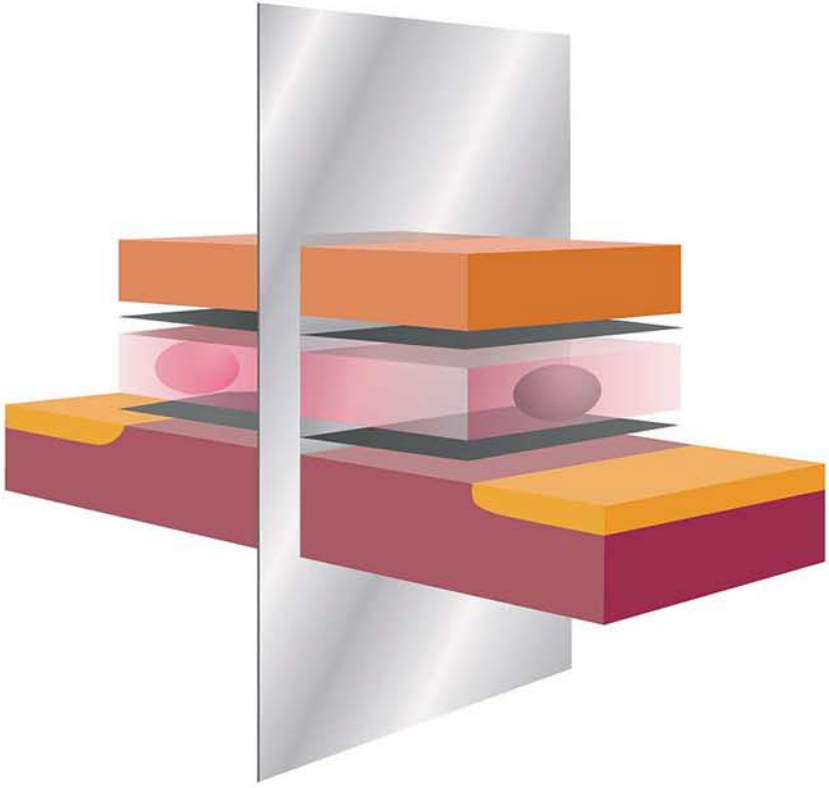
AMD

MirrorBit™



Reliability Study

AMD FLASH MEMORY

AMD MirrorBit™

RELIABILITY STUDY

White Paper

OVERVIEW

The MirrorBit™ cell is a breakthrough in NOR Flash memory cell architecture that enables a Flash memory product to hold twice as much data as standard Flash, without compromising device endurance, performance or reliability.

The MirrorBit architecture is the result of years of research and development on the design, processing, testing and characterization of multi-bit cells that has culminated in AMD's patented MirrorBit architecture. MirrorBit memory cells, which store a full charge in each of two physically distinct locations, offer many advantages over MLCs that store fractional levels of charge in one location. Since each bit in the MirrorBit memory cell is physically in a different location, the bits are independent and do not interact with each other, allowing AMD to offer the same performance and reliability as standard single-bit Flash memory products.

Over 350 billion MirrorBit memory bits have been tested and studied since the inception of this technology. Over six thousand devices and packages were subjected to extensive tests for qualification of MirrorBit technology. This extensive testing is testament of AMD's commitment to delivering highly reliable and world-class quality on of all its products. Over one billion bits have also been characterized through 100,000 read-program-erase cycles.

Reliability testing allows AMD to offer MirrorBit devices that are designed to deliver 100,000 program/erase cycles, as well as 20 years of data retention at 125°C. Testing shows that failure rates are consistent with AMD's standard floating gate technology. Furthermore, we expect to complete characterization of endurance at the 1M cycle level in the near future.

The focus of this article is to explain the methodology and testing employed to characterize and qualify the reliability of MirrorBit based Flash products.

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WHAT IS RELIABILITY?

Reliability can be defined as the ability of a product to perform its stated functions for a predictable length of time. Failure is loss of ability of a device to perform any of its required functions.

There are two basic categories of device failure that can affect reliability. Hard failures, or complete and unrecoverable faults in the device, arise from defects that occur during the manufacturing process. Once there is a hard failure, the device fails and it cannot be recovered. On the other hand, soft failures occur over time as a result of operating the device and are caused by physical degradation of the device. These types of failures can be recovered. However, either type of failure results in reduced reliability.

Reliability is tested for and ensured by accelerated stress tests. A well-designed stress test quickly identifies the relevant failure mechanism. The advantages of accelerated stress testing are that these tests stress the device in order to bring out low-rate failures. They also make it possible to replicate failures that would occur over many years of device operation in a large population by using a smaller sample population over a shorter time but with accelerated stress. Once the problem is identified, either the root-cause is eliminated or a screen is implemented to ensure that the failure is contained.

A number of different stress tests have been used to help ensure that MirrorBit products offer high levels of endurance, reliability and data retention. The attached flowchart (Figure 1) summarizes the reliability stress tests (product and package tests) performed to qualify the MirrorBit technology. Test results summarized in this study are included in the Am29LV640MU/Am29LV641MH/L Qualification Summary.

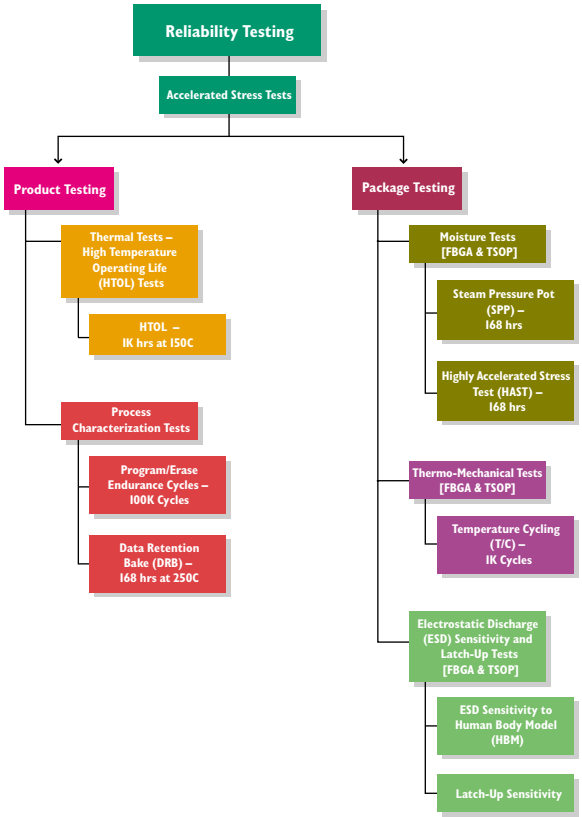
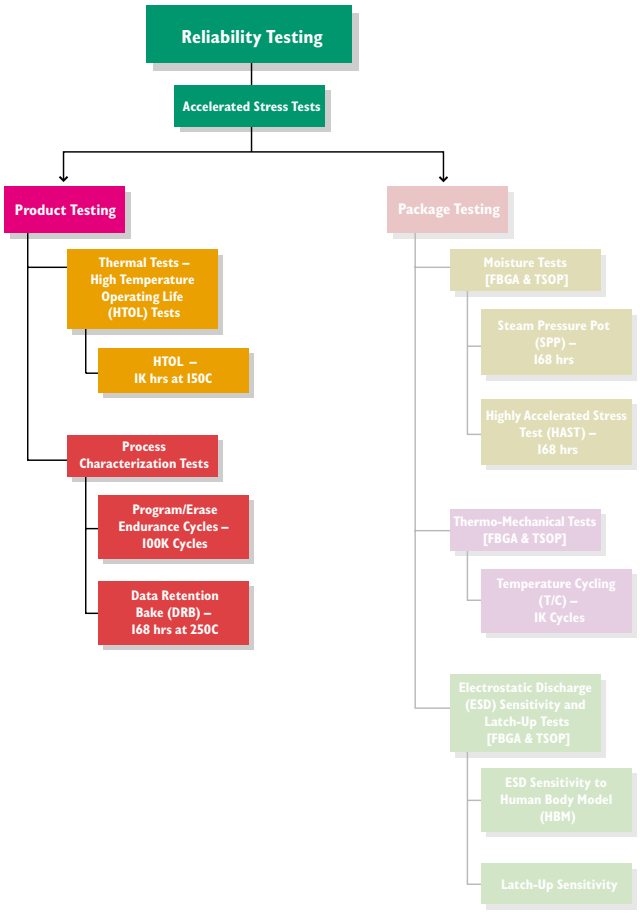


Figure 1



Flash memory device testing comprises of tests such as

1. High Temperature Operating Lifetest (HTOL)
2. Program/Erase Cycling (Endurance)
3. Data Retention Bake (DRB) tests

These tests help ensure that

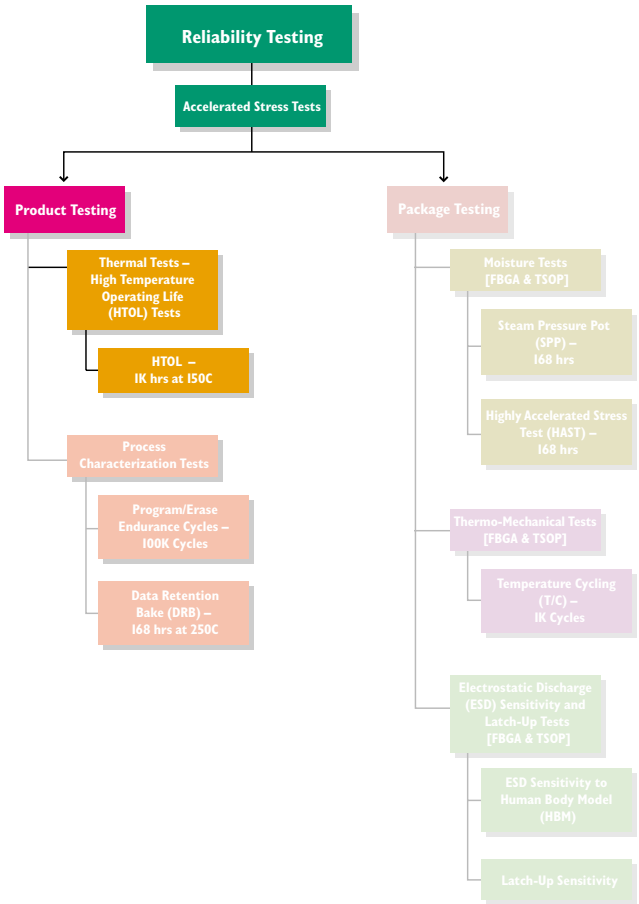
- devices shipped will not fail in the field at unacceptable rates
- devices shipped will meet the industry's highest endurance specification of 1,000,000 program/erase cycles (100,000 initially)
- devices shipped will retain data for more than 20 years at 125°C

High Temperature Operating Life (HTOL) tests help ensure that the product performs reliably, both upon receipt of shipment as well as in the end system. Accelerated thermal tests are used by AMD to:

- Ensure that the rate of failure in the field is very low and within acceptable levels
- Provide an estimate of the operating life and field failure rate of a device

Thermal tests performed to qualify MirrorBit devices are:

- High Temperature Operating Life (HTOL)
  IK hours at 150°C data
- MirrorBit technology achieves the same results as AMD's standard floating gate technology



Reliability studies have shown that the probability of a generic device failure in the field is as shown in Figure 2.

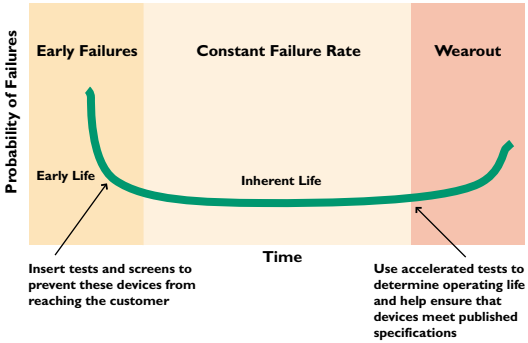


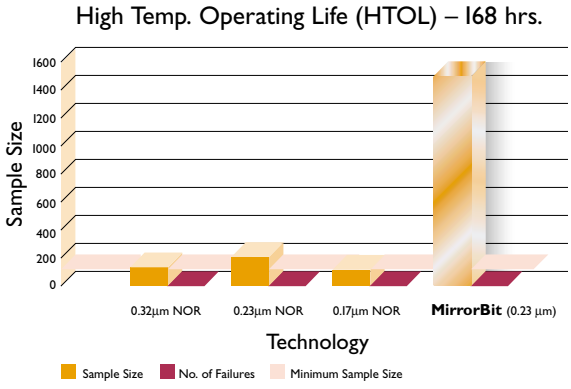
Figure 2 Bathtub Curve

Operating life tests are performed while the device is under power and functioning as intended, and are used to elucidate the various failure mechanisms intrinsic to the manufacturing process.

HTOL test comprises tests to check for Early Life/Infant Mortality, Inherent Life and Wearout Region functionality of MirrorBit devices.

Early Life / Infant Mortality in the HTOL test is used to weed out any failures early in the device's life. The purpose of the Early Life (EL) test is to detect and quantify the presence of failure mechanisms that occur due to a "defective subpopulation". This portion of the total device population has generally been affected by some anomalous condition during manufacturing.

The early life failure rate enables us to estimate the time to first failure for this product. This test also helps us to implement screens to prevent early life fallout in the future (e.g., screen to repair slow erase bits in the population).



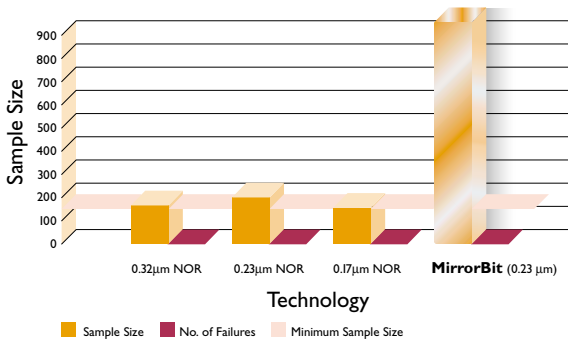
Early Life/Infant Mortality Test	
Temperature	150°C
Duration	168 hours
Voltage	3.6V
Number of lots tested	3
Devices tested	1443
Maximum estimated failure rate	350 FITS
Calculated failure rate	51 FITS
Failures	0
Pass/Fail	**PASS**

Inherent Life (Constant Failure Rate) test is designed to detect failure mechanisms that are intrinsic to the entire population of devices. This test provides an estimate of the failure rate beyond the early life period. The Bathtub curve (Figure 2) shows this as the constant failure rate region and is used to determine the "useful or working life" of the devices.

Results from the accelerated conditions are translated to standard application conditions using the appropriate data models and activation energies in order to estimate the field reliability in FITS (Failures in Time)[1] of the product.

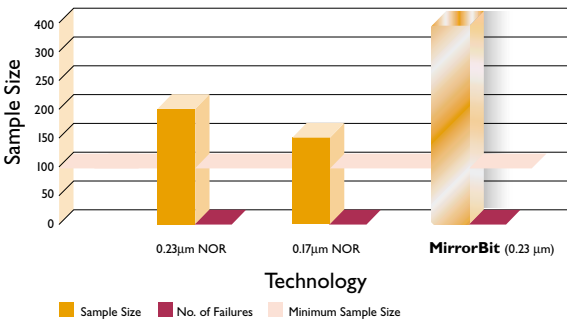
Wearout Region of the HTOL test demonstrates a rapidly increasing failure rate. It is not generally observed for today's integrated devices (obsolescence).

High Temp. Operating Life (HTOL) – 500 hrs.



Inherent Life /Constant Failure Rate	
Temperature	150°C
Duration	500 hours
Voltage	3.6V
Number of lots tested	3
Devices tested	961
Maximum estimated failure rate	150 FITS
Calculated failure rate	6 FITS
Failures	0
Pass/Fail	**PASS**

High Temp. Operating Life (HTOL) – 1000 hrs.



Inherent Life /Constant Failure Rate	
Temperature	150°C
Duration	1000 hours
Voltage	3.6V
Number of lots tested	2
Devices tested	399
Maximum estimated failure rate	150 FITS
Calculated failure rate	6 FITS
Failures	0
Pass/Fail	**PASS**
MTTF (Mean time to failure)	19,026 years

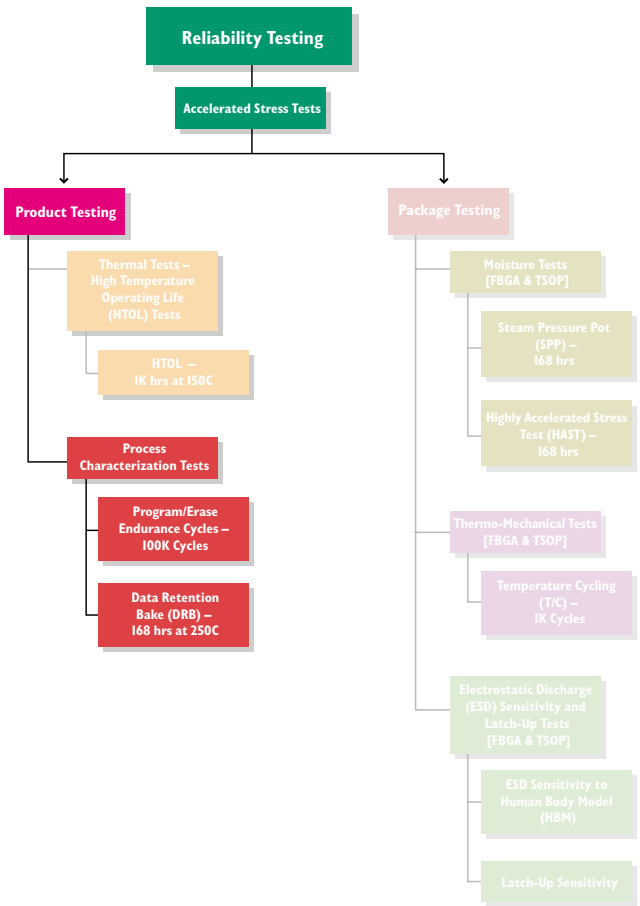
Note:
1. The FIT failure rate is expressed in number of failures per billion hours.

Process Characterization tests confirm that the process and the device have been characterized over the specified range of process variations, using silicon from the production Fab. These tests are performed to help ensure that:

- Devices shipped will meet the industry's highest endurance specification of 1,000,000 program/erase cycles (100,000 initially)
- Devices shipped will retain data for more than 20 years at 125°C

Tests performed to qualify MirrorBit devices are:

- Program/Erase Endurance Cycles **100K cycles data (Further testing underway to 1M cycles)**
- Data Retention Bake (DRB) **168 hours at 250°C data**
- MirrorBit products exhibit the same high levels of endurance and data retention as standard AMD Flash.



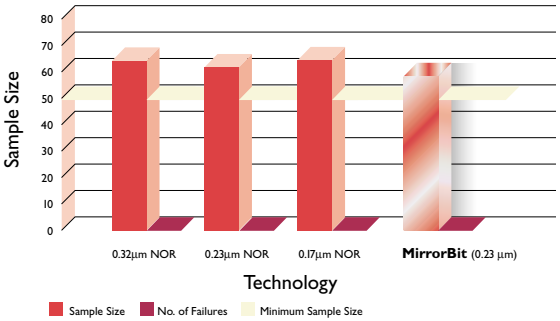
In addition to data retention, the other important requirement for Flash memory integrity is endurance. Endurance, or the ability to repeatedly program and erase a memory cell, is closely connected with the reliability of the cell.

Program/Erase endurance cycling tests are performed to help ensure that the device is able to sustain repeated data changes (P/E cycles). MirrorBit Flash devices were placed on boards and biased in thermal chambers set at high and low temperatures. The components were cycled repeatedly through programming and erase conditions. Margin verification was automatically performed after each cycle.

Endurance failures are caused predominantly by charge trapping or oxide rupturing occurring in the charge transfer dielectric (e.g., via tunneling, hot electrons) during program/erase cycles [1]. The test is also used to check for any charge loss/gain issues and erase time degradation issues with the device.

These tests help make sure that MirrorBit devices currently meet the 100,000 cycles threshold, and that they can eventually meet the industry's highest endurance specification of 1,000,000 program/erase cycles set by AMD.

Program/Erase Endurance – 100K cycles Matrix[1]



Endurance	
Temperature	-40°/25°/90°C
Duration	100K cycles
Number of lots tested	1
Devices tested	57
Failures	0
Pass/Fail	**PASS**
Specified Endurance	100K cycles[2]

Note:

1. Tempture/Voltage stress conditions used to test MirrorBit devices are included in the Am29LV640MU/Am29LV641MH/L Qualification Summary.
2. Units undergoing further testing to 1M cycles.

The most fundamental requirement for Flash memory, or any non-volatile memory, is that of data retention. Any Flash memory solution should guarantee a period over which data will be retained by the device. It is important to realize that data retention is strongly dependent on temperature. All AMD Flash memory devices, including MirrorBit Flash devices, are specified to retain data for 20 years at 125°C.

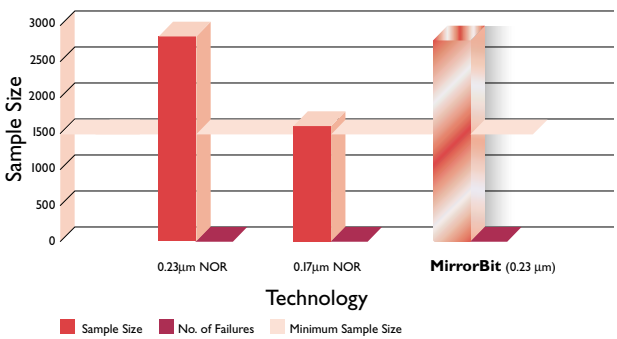
Data retention is essentially a process of trapping or confining electrons in the charge storage medium. Mechanisms for electron gain/loss, (i.e., transport to/from the dielectric), follow basic chemical kinetics. The rate of these phenomena is described by the Arrhenius equation[1] and is exponentially dependent on temperature. As a result, AMD explicitly states both time and temperature while specifying data retention.

Data Retention Bake (DRB) test is used to characterize the ability of the Flash memory device to retain the appropriate level of charge. Any charge gain/loss is caused by defects in either the charge storage material or select gate oxide. Abnormal levels of charge gain/loss can result in a change in the number of electrons in the storage dielectric, and therefore compromise data integrity. AMD's data retention bake test helps ensure that devices shipped to the customer offer the highest levels of data integrity.

The DRB testing is performed by loading a test pattern into a wafer and then baking the wafer for 168 hours at 250°C. The baked devices are submitted to a number of electrical tests, and the post-test memory pattern must be identical to the pre-test pattern, for the devices to pass.

Testing for data retention baked for 168 hrs. at 250°C equates to a lifetime of more than 20 years at 125°C.

Wafer Level Data Retention Bake (DRB) – 168hrs. 250°C

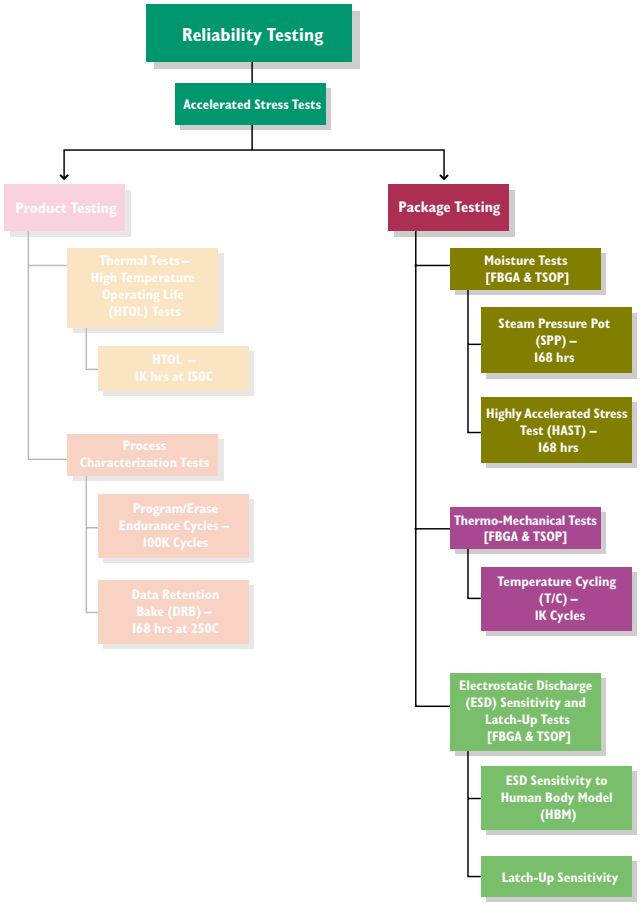


Data Retention Bake (DRB)	
Temperature	250°C
Duration	168 hours
Number of lots tested	1
Devices tested	2603
Failures	0
Pass/Fail	**PASS**
Specified Data Retention	20 years at 125°C

Note:

1. The Arrhenius equation is expressed as: $R_1=R_0\exp^{(-E_a/kT_1)}$

Where: R_1 = Reaction Rate; R_0 = A Constant; E_a = Activation energy; k = Boltzman's Constant (8.62×10^{-5}eV/°K); T_1 = Reaction Temperature (°K)



PACKAGE LEVEL TESTING INCLUDES:

1. Steam Pressure Pot (SPP) test
2. Highly Accelerated Stress Test (HAST)
3. Temperature Cycling (T/C)
4. Electrostatic Discharge (ESD)
5. Latch-up sensitivity tests

Package level tests check for issues such as:

- molding problems
- chemical/galvanic corrosion of the metallization
- moisture penetration
- temperature induced stress cycles
- cracking of the die/package
- electrostatic shocks

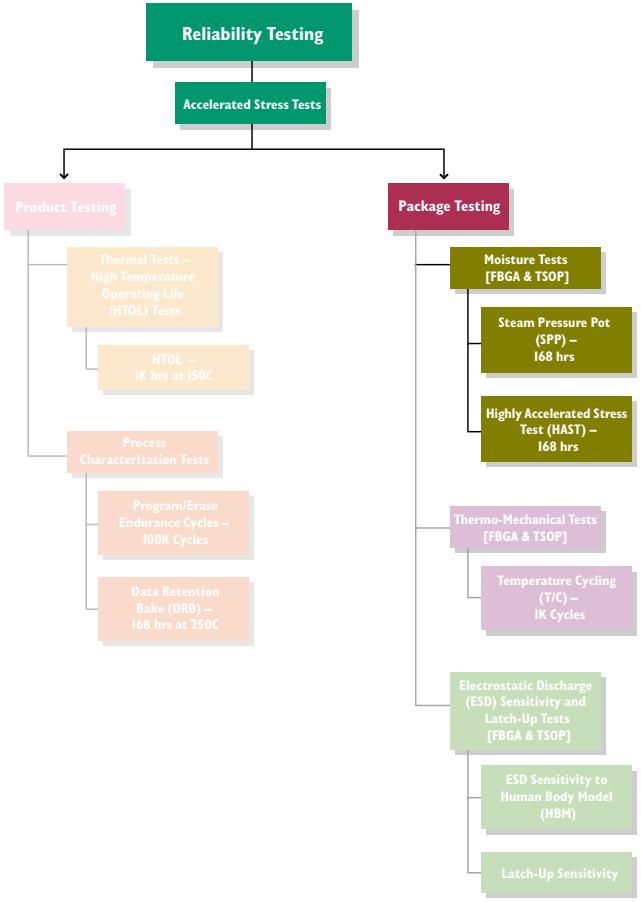
Moisture tests are designed to assess the ability of packaged parts to withstand moisture contamination. These tests reveal:

- Problems with die/package combination
- Problems with molding process
- Any chemical or galvanic corrosion of the die metallization
- Other moisture and contamination related failure mechanisms

Two moisture tests used to help ensure that MirrorBit devices can be used in a system that may be powered on and off in a high humidity environment are:

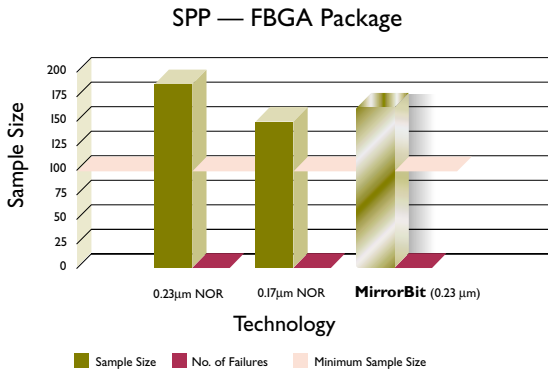
- Steam Pressure Pot (SPP) **168 hours data**
- Highly Accelerated Stress Test (HAST) **168 hours data**

- Results from the above tests show that packaged MirrorBit products have the same level of reliability as standard AMD Flash.

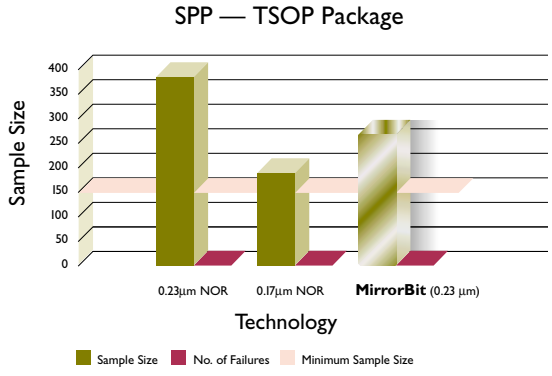


Steam Pressure Pot (SPP) testing is used to evaluate plastic package survivability when moisture is forced through the encapsulant to the die surface. Packaged MirrorBit devices were placed in pressurized chambers and exposed to saturated steam at 121°C and pressure of 15 psig for 168 hours.

This test is designed to be an indicator of any gross problems with the die/package combination or with the molding process. The test is primarily used to check for moisture and contamination related failure mechanisms. The test also checks for any chemical or galvanic corrosion[1] of the die metallization.



Steam Pressure Pot (FBGA)	
Temperature	121°C
Duration	168 hours
Humidity	Saturated Steam
Pressure	15 psig
Number of lots tested	3
Devices tested	165
Failures	0
Pass/Fail	**PASS**



Steam Pressure Pot (TSOP)	
Temperature	121°C
Duration	168 hours
Humidity	Saturated Steam
Pressure	15 psig
Number of lots tested	5
Devices tested	274
Failures	0
Pass/Fail	**PASS**

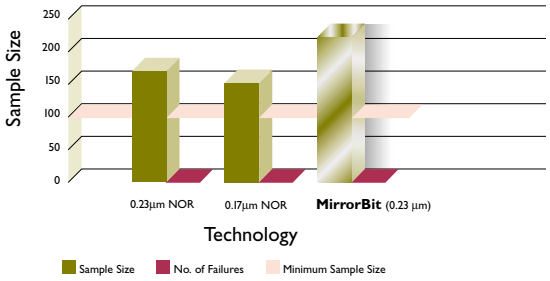
Note:
1. Galvanic couple formed by gold ball bond on aluminum provides driving force to accelerate corrosion.

Highly Accelerated (Temperature and Humidity) Stress Test (HAST) is performed for the purpose of evaluating the reliability of non-hermetic packaged solid-state devices in humid environments [2]. It employs severe conditions of temperature, humidity and bias, which accelerate the penetration of moisture through the external protective material (encapsulant or seal) as well as the interface between the encapsulant/seal and the metallic conductors.

MirrorBit Flash devices were mounted on boards with a DC bias applied to the parts. The boards were placed in a pressurized test chamber at a relative humidity of 85% and at temperatures between 110°C to 150°C. Intermediate electrical test readouts were taken with the final readout at 168 hours.

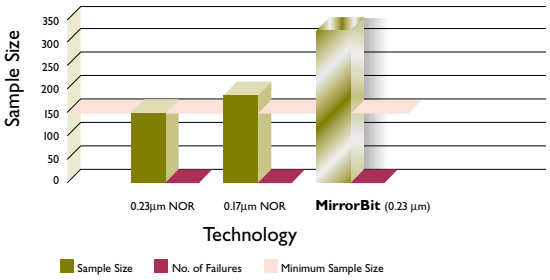
The stress usually activates the same failure mechanisms as the "85/85" Steady-State humidity Life Test (JEDEC Standard No. 22-A101).The test assumes moisture penetration to the die surface and that the primary failure mechanism will be electrolytic corrosion of the die metallization[1]. Other moisture and contamination related failure mechanisms might also be observed. The test is intended to evaluate the molding compound purity, as well as the quality of the passivation and glassivation processes.

HAST — FBGA Package



Highly Accelerated Stress Test (FBGA)	
Temperature	110-150°C
Duration	168 hours
Relative Humidity	85%
Number of lots tested	4
Devices tested	217
Failures	0
Pass/Fail	**PASS**

HAST — TSOP Package



Highly Accelerated Stress Test (TSOP)	
Temperature	110-150°C
Duration	168 hours
Relative Humidity	85%
Number of lots tested	6
Devices tested	335
Failures	0
Pass/Fail	**PASS**

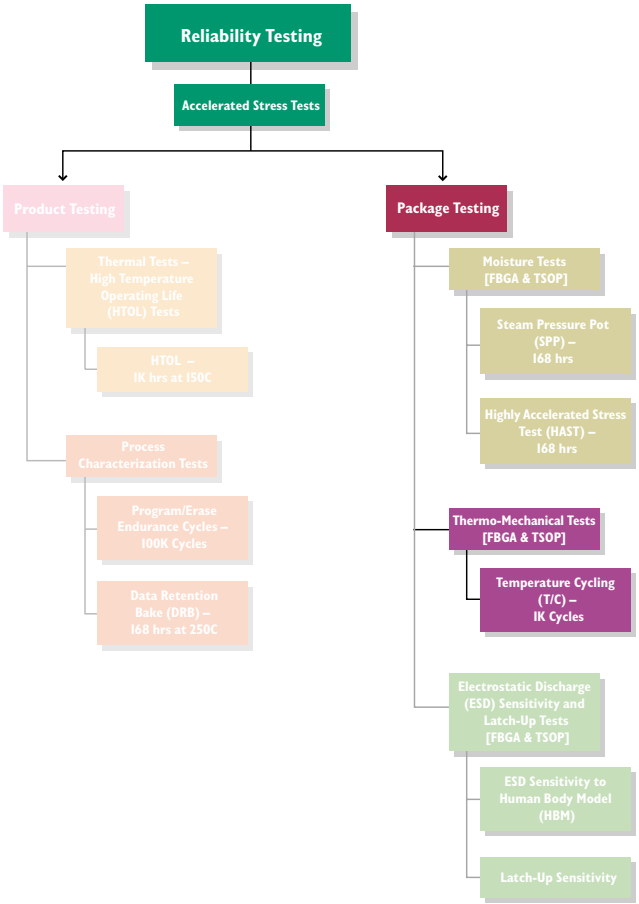
Note:
1. An electrochemical reaction that consumes metallization and results in loss of contact and function.

Thermo-Mechanical Tests:

- Cycle a package between high and low temperature extremes, causing mechanical stresses in the packaged device
- Are used to help ensure that there are no failures due to the mismatch of coefficients of thermal expansion, or mechanical or manufacturing defects

Test performed to qualify MirrorBit devices:

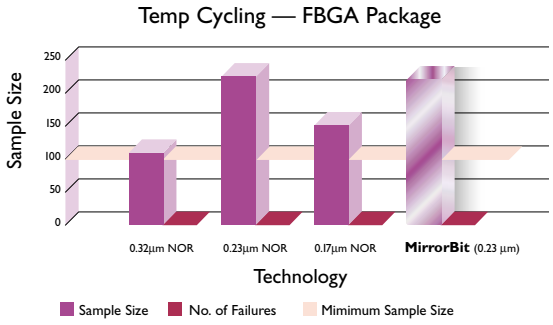
- Temperature Cycling (T/C)
  IK cycles data
- Results show that packaged MirrorBit devices demonstrate the same levels of reliability as standard AMD flash.



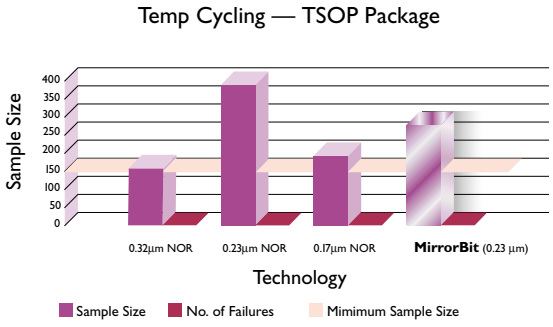
Temperature Cycling (T/C) testing cycles a package between high and low temperature extremes. Through continuous cycling from high to low temperatures, the structure expands and contracts, causing mechanical stresses in the packaged device.

MirrorBit devices were placed in chambers that automatically cycle between air temperatures as low as -40°C and as high as 150°C. Standard temperature ranges as well as dwell times followed JEDEC Standards. The final readpoint for this test was at 1K cycles.

This test is especially useful for detecting stress-induced failures from the mismatch in coefficients of thermal expansion for the die/package structure.



Temperature Cycling (FBGA)	
Temperature	-40°C to 150°C
Cycles	1000
Number of lots tested	4
Devices tested	219
Failures	0
Pass/Fail	**PASS**



Temperature Cycling (TSOP)	
Temperature	-40°C to 150°C
Cycles	1000
Number of lots tested	5
Devices tested	274
Failures	0
Pass/Fail	**PASS**

- ESD (Electrostatic Discharge) sensitivity testing helps ensure that the product is robust enough to survive normal assembly handling by the customer. The objective is to minimize failures resulting from human or equipment handling

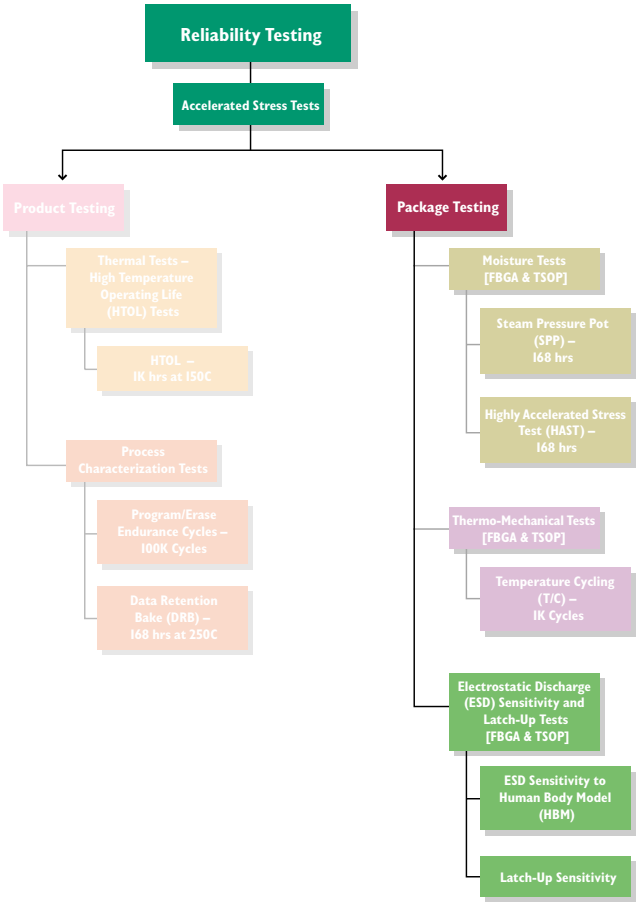
- Latch-Up (LU) evaluation is to minimize EOS (electrical overstress) failures due to latch-up during test, burn-in and in end-use systems

ESD Sensitivity and Latch-up Tests:

- ESD Sensitivity to Human Body Model (HBM)
  Passes 4000V

- Latch-Up Sensitivity
  Results: Pass

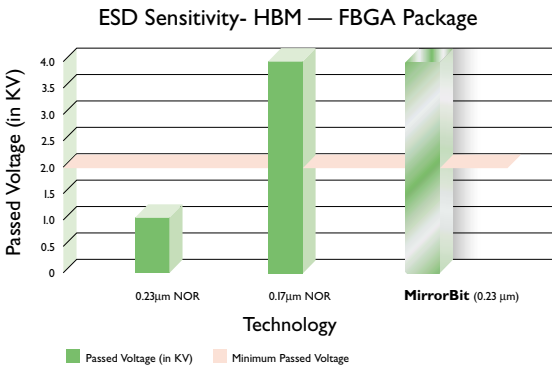
- MirrorBit products exhibit equivalent or better ESD and Latch-up characteristics than standard AMD Flash.



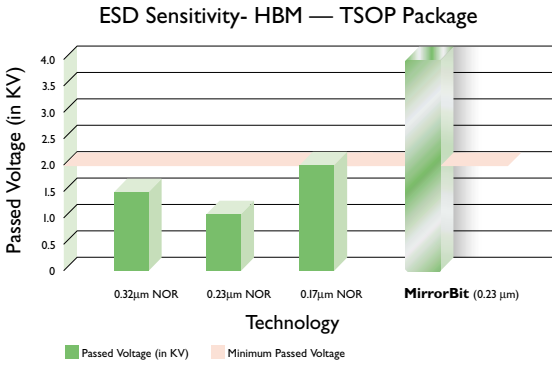
The historic method of classifying components for ESD Susceptibility uses the Human Body Model. The discharge waveform is intended to approximate the ESD event from a human finger to a pin of the component while other pins are at ground potential. Products must display a HBM Withstand Voltage > +/- 2000 volts nominal to pass qualification requirements.

A charging voltage of +/- 1000, 2000, 3000, and 4000 volts nominal was applied to the device and discharged separately to each pin-pair combination. The stress applied consisted of 3 positive pulses followed by 3 negative pulses. The test procedure and discharge waveform are specified in ANSI/ESD S-5.1.

This test checks for any electrical failures such as increased leakage currents as well as ESD damage at I/O's or in the die core.



ESD Sensitivity to HBM (FBGA)	
Temperature	Ambient
Voltage applied to each pin pair	+/- 1kV, 2kV, 3kV, 4kV
Minimum voltage required to pass test	2000V
Actual test voltage passed	>4000V
Number of lots tested	36
Devices tested	180
Failures	0
Pass/Fail	**PASS**



ESD Sensitivity to HBM(TSOP)	
Temperature	Ambient
Voltage applied to each pin pair	+/- 1kV, 2kV, 3kV, 4kV
Minimum voltage required to pass test	2000V
Actual test voltage passed	>4000V
Number of lots tested	12
Devices tested	60
Failures	0
Pass/Fail	**PASS**

Note: Results for HBM show a greater than 100% improvement in ESD sensitivity when compared to standard floating gate technology.

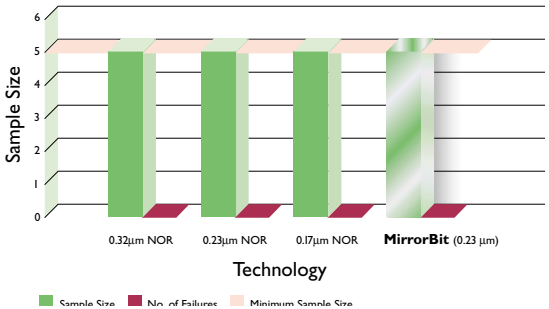
Latch-up can occur when a sustained low impedance path is created between the power supply rails. This is caused by triggering parasitic 4 layer bipolar structures (SCR) by current generated from various sources. SLU test method is used to assess product susceptibility to latch-up.

An over-voltage is forced on each supply pin and a trigger current is forced on the I/O pins in valid logic states at 125°C. Trigger polarity is chosen to result in an overstress condition. The long slow trigger pulse conforms to JEDEC Std-17 to eliminate any transient effects.

For qualification, products were required to display a PS Withstand Voltage of Vcc max + 2.0 volts on power supply pins. I/O Withstand Currents greater than +100ma @ Vcc max + 3.0 volts and greater than -100ma @ Vss - 2.0 volts.

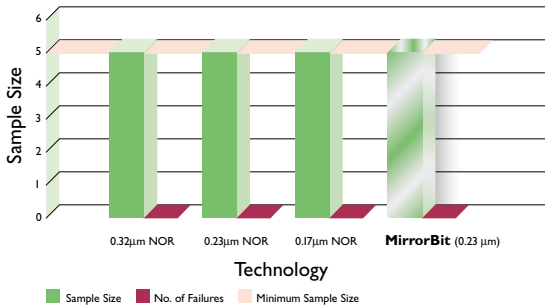
This test is used to detect failures caused by any electrical failure or Latch-up condition. Any form of EOS[1] damage to the package or the die can be detected.

Latch-Up Test—FBGA Package



Static Latch-up Sensitivity (FBGA)	
Temperature	125°C
Voltage applied	5.6V
Minimum current allowed to pass test	+/- 100mA
Number of lots tested	1
Devices tested	5
Failures	0
Pass/Fail	**PASS**

Latch-Up Test—TSOP Package



Static Latch-up Sensitivity (TSOP)	
Temperature	125°C
Voltage applied	5.6V
Minimum current allowed to pass test	+/- 100mA
Number of lots tested	1
Devices tested	5
Failures	0
Pass/Fail	**PASS**

Note:
1. Electrical Overstress

[1]: Jedec Standard EEPROM Program/Erase Endurance and Data Retention Test JESD22-A117

[2]: EIA/Jedec Standard Test Method JESD22 A110-B; Highly Accelerated Temp. & Humidity Stress Test (HAST)

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