Chapter 2 Package Design

SURFACE-MOUNT ARRAY PACKAGES

In the last several years, the growth in the world-wide usage of surface-mount array packages has been tremendous. The benefits that have helped spur this growth include:

- Less board space required.
- Compatibility with the same surface-mount board assembly process as quad flat packages.
- High board assembly yields due to the self-aligning nature of the solder balls to the corresponding land pads during the solder reflow process.
- Enhancements to package electrical performance due to increased flexibility in the package design:
  - More flexibility in routing of traces, allowing better control of the lengths of critical signal lines.
  - Option of having extra planes for power distribution, which lowers inductance, thereby reducing noise.

The primary trade-off to using surface-mount array packages is encountered after board assembly because once mounted, no rework of the individual solder joints is possible the way it is with leaded packages. Instead, the package is removed from the board, the land pattern redressed, and a new part is applied. Detecting these assembly defects is done via electrical performance tests because X-ray inspection of the solder joints is simply too expensive. Fortunately, board assembly yields are proving to be so high that this trade-off is not affecting the popularity of these packages.

AMD offers surface-mount array packaging in the following families:

- Organic Ball Grid Array Packages (OBGAs) (flip-chip)
- Plastic Ball Grid Array Packages (PBGAs) (wirebond)
- Ceramic Column Grid Array Packages (CCGAs)

Organic Ball Grid Array. The use of organic materials in packages is becoming more popular for a variety of reasons, including improved electrical performance. Additionally, the coefficient of thermal expansion (CTE) of organic packages and printed circuit boards are more closely matched, hence the reliability of the solder ball interconnection is greatly improved.

An OBGA package typically consists of "build" up layers instead of laminated layers as found in traditional PBGA packages. It is a die-down configuration where the interconnections are formed using flip-chip technology with C4 solder bumps instead of conventional wirebonding. Solder bumps are fabricated on the bond pads on the die, and reflowed during assembly to form a bond with a corresponding land pattern of solder pads on the substrate. Traces from these interconnections routed through the substrate to solder balls on the backside of the package body are used as the outer connections to the printed circuit board.

The table on *page 2-3* provides an overview of each device within the OBGA package family.

Package Attributes: Organic Ball Grid Array

Package Code/Ballcount	OBF 349	OLF 564	OLF 829
JEDEC Drawing #	N/A	N/A	N/A
Package Body Size (L x W) (basic, mm)	25.0 x 25.0	30.0 x 30.0	37.5 x 37.5
Ball Pitch (mm)	1.27	1.27	1.27
Package Body Thickness (maximum, mm)	1.13	1.1	1.2
Package Height (includes standoff) (maximum, mm)	2.61	3.56	3.67
Coplanarity (mm)	0.20	0.20	0.20
Lead Formation	Solder balls	Solder balls	Solder balls
Package Weight (grams)	Note[3]	Note[3]	Note[3]
Product Carrier[1]	Tray	Tray	Tray
JEDEC Moisture Sensitivity Rating[2]	4	4	4
UL Flammability Rating and Oxygen Index	94 V-0 and ≥ 28%	94 V-0 and ≥ 28%	94 V-0 and ≥ 28%

Note:

1 See *Chapter 7 Trays* for further information.

2 See *Chapter 12 Dry Packing* for further information.

3 Contact your AMD sales representative for this data.

Plastic Ball Grid Array. For high I/O devices, the plastic BGA (PBGA) is a popular alternative to the larger form/fit QFP. The PBGA fulfills the need for high-performance, high-density packaging in a format that can be readily accommodated with existing surface-mount assembly equipment. The supporting infrastructure for PBGAs is now established, with industry standards established for both the JEDEC package outline and the IPC land pattern for BGA.

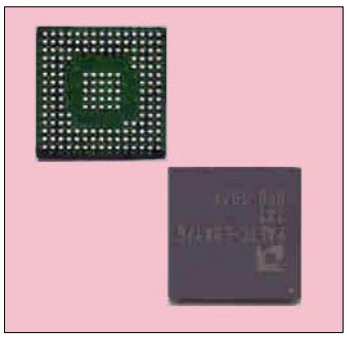

Figure 2.1 Plastic Ball Grid Array Package

The PBGA package consists of a substrate made of a high-temperature epoxy laminate. It is overlaid with copper over which metallized wire bond pads and a die pad are fabricated. The wire bond pads extend outward to plated through-hole vias in the package. The vias provide the electrical continuity from the top of the package to the other side, where they connect to copper traces that run from the holes to a matrix of solder bumps. The bumps are soldered onto a matching land pattern on the circuit board in the end-use application. A solder mask is photo defined on the backside of the package to contain the flow of solder during board assembly.

The die is attached to the die pad using a standard epoxy die attach method. Gold ball bonding is used to connect the die pads to the wirebond pads, and the die of overmolded with silicone-modified, epoxy novolac encapsulation material to protect it.

Variations in the PBGA package design include cavity-up or cavity-down configurations, along with thermally enhanced versions (with heat sinks or thermal vias). The PBGA can also be designed to accommodate multiple chips inside, enabling more complete silicon solutions in a single IC package.

For easy comparison between the different PBGA packages, the table starting on *page 2-5* provides an overview of each device within the PBGA package family. Details on the material content of select PBGA packages can be found in *Chapter 4 Package Materials*.

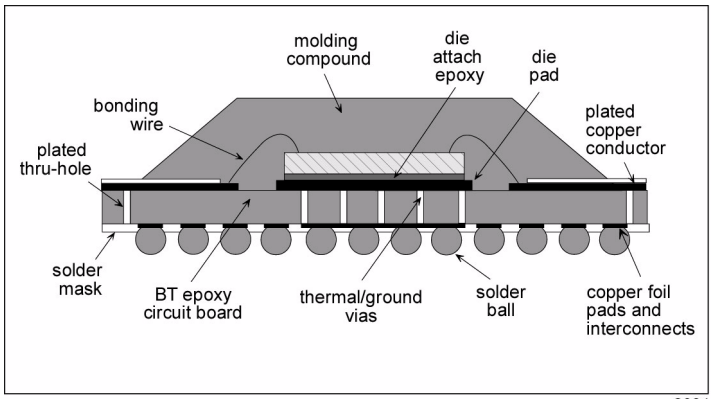

Figure 2.2 Cross-section of plastic ball grid array package.

Package Attributes: Plastic Ball Grid Array

Package Code/Ball count	BGA 492
JEDEC Drawing#	MS-034 (A)/Bar-2
Package Body Size (L x W) (basic, mm)	35.00 x 35.00
Ball Pitch (mm)	1.27
Package Body Thickness (nom, mm)	1.73
Coplanarity (mm)	0.20
Lead Formation	Solder balls
Package Weight (grams)	4.61
Product Carrier[2]	Tray 13’ Tape & Reel
JEDEC Moisture Sensitivity Rating[3]	4
UL Flammability Rating and Oxygen Index	94 V-0 and ≥28%

Notes:

1. Depending on the assembly location, the encapsulation could be globtop, which would increase the maximum package body thickness to 1.91 mm, and the package height to a maximum of 2.61 mm.

COLUMN GRID ARRAY PACKAGES

As the demand for devices with increasingly greater numbers of interconnections grows, the popularity of the column grid array package also grows. The design of this package is similar to a BGA except that a round post, instead of a ball, is used for the attachment contact.

Ceramic Column Grid Array.

AMD's ceramic column grid array (CCGA) package is seen as an alternative for the ceramic BGA package for applications requiring a larger number of interconnections. Additionally, the column structure of the CCGA package provides improvement to the thermal fatigue life of the package solder joint for many applications. The supporting infrastructure for CCGAs has been established for both the JEDEC package outline and the IPC land pattern.

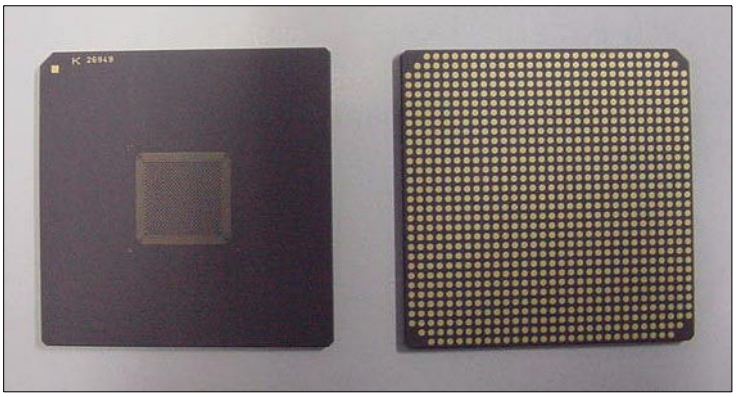

Figure 2.3 Ceramic Column Grid Array Package (shown without interposer)

The CCGA package is made from ceramic-based material used in the traditional BGA package. The CCGA package uses flip-chip technology as the means for forming interconnections. It also has an interposer with a lid over the die for heat distribution.

The table on *page 2-9* provides an overview of each device within the CCGA package family.

Package Attributes: Ceramic Column Grid Array

Package Code/Ballcount	CCF 575	C2F 949
JEDEC Drawing #	N/A	N/A
Package Body Size (L x W) (basic, mm)	30.00 x 30.00	40.00 x 40.00
Pitch (mm)	1.27	1.27
Package Body Thickness (maximum, mm)	1.137	1.522
Package Height (includes standoff) (maximum, mm)	3.865	5.257
Coplanarity (mm)	0.15	0.20
Lead Formation	Columns	Columns
Package Weight (grams)	Note[2]	Note[2]
Product Carrier[1]	Tray	Tray
JEDEC Moisture Sensitivity Rating	N/A	N/A
UL Flammability Rating and Oxygen Index	N/A	N/A

Note:

1 See *Chapter 7 Trays* for further information.

2 Contact your AMD sales representative for this data.

THRU-HOLE PACKAGES

Thru-hole package designs have been around since the early 1960s and continue to enjoy popularity despite the emergence of surface-mount devices.

AMD offers the following thru-hole package families:

- Pin Grid Array (PGA)
  - Ceramic Pin Grid Array (CPGA)
  - Ceramic Micro Pin Grid Array (CµPGA)
  - Organic Pin Grid Array (OPGA)
  - Organic Micro Pin Grid Array (OµPGA)
- Dual-in-Line (DIP)
  - Plastic Dual-in-Line (PDIP)

Ceramic thru-hole package designs are used extensively in applications where fail-safe product reliability is required. Compared to plastic materials, ceramic package materials offer superior performance in hermeticity, high-temperature stability, and electrical and thermal conductivity. The use of organic materials in packages is becoming more popular for a variety of reasons, including improved electrical performance.

Ceramic Pin Grid Array. AMD designs its CPGA packages using flip chip interconnection.

***Package Design*—**With flip-chip technology, solder is used instead of wire to provide the metallurgical means for forming interconnections. Solder is applied to the bond pads and the die is "flipped" over and interconnected to the package base. Because the bond pads can be placed in an array on the active area of the die instead of around the die's perimeter, the flip-chip process offers the following advantages over the conventional wire bonding process:

- Greater number of available pins
- Smaller die size
- Shortened electrical connections (thus improved electrical performance)
- Increased manufacturing efficiency

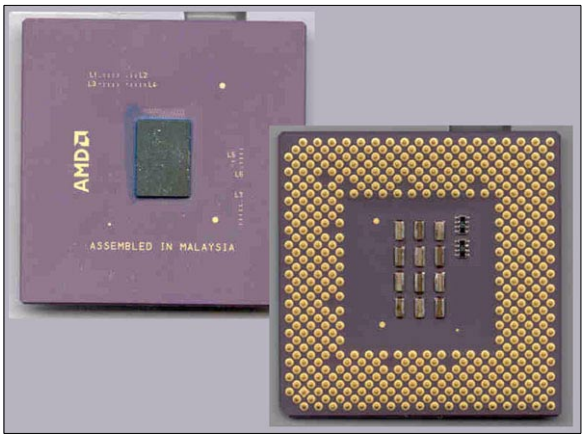

Figure 2.10 Sample of AMD's CPGA package.

The table beginning on *page 2-25* provides an overview of each package style within the CPGA package family and contains such information as dimensioning data along with package weight and available product carriers. For details on the material content of each individual package, see *Chapter 4 Package Materials*.

Package Attributes: Ceramic Pin Grid Array

Package Code/Pin Count	CGF 321	CGF 453
Package Body Size (L x W) (nom)	1.95 x 1.95 in.	49.53 X 49.53 mm
Pin Pitch	0.050 in.	1.27 mm
Package Body Thickness (to baseplane)[1] (nom)	0.056 in.[1]	1.4 mm[1]
Package Height[2, 3]	0.239 in. (nom)[2]	6.74 mm (max)[3]
Coplanarity	N/A	N/A
Package Weight (grams)	21.2	17.4
Product Carrier[4]	Tray	Tray
JEDEC Moisture Sensitivity Rating	N/A	N/A
UL Flammability Rating and Oxygen Index	N/A	N/A

Notes:

1 Refers to substrate thickness only.

2 Includes standoff, substrate and lid.

3 Includes standoff, substrate, chip, and pad.

4 See *Chapter 7 Trays* for further information.

Ceramic Micro Pin Grid Array. The demand for smaller package sizes, as well as for increased pin counts, has resulted in the development of ceramic micro-PGA packages.

Package Design—The pin arrangement on AMD's CμPGA package is more densely packed than that which is found on conventional CPGA packages, thus resulting in a smaller package size. AMD designs its CμPGA packages using flip chip interconnection.

AMD currently offers a 940 pin count in this package style (UCG 940). The table below provides an overview of this device. For details on the material content of each individual package, see *Chapter 4 Package Materials*.

Package Attributes: Ceramic Micro Pin Grid Array

Package Code/Pin Count	UCG 940
Package Body Size (L x W) (nom, mm)	40.00 x 40.00
Pin Pitch	1.27
Package Body Thickness (to baseplane)[1] (nom, mm)	1.67[1]
Package Height[2] (nom, mm)	7.04[2]
Coplanarity	N/A
Package Weight (grams)	Note[4]
Product Carrier[3]	Tray
JEDEC Moisture Sensitivity Rating	N/A
UL Flammability Rating and Oxygen Index	N/A

Notes:

1 Refers to substrate thickness only.

2 Includes standoff, substrate and lid.

3 See *Chapter 7 Trays* for further information.

4 Contact your AMD sales representative for this data.

Organic Pin Grid Array. Cost and performance issues are two of the driving factors behind AMD developing packages made with organic materials.

***Package Design*—**AMD's organic pin grid array (OPGA) package utilizes the flip-chip interconnection design style. With flip-chip technology, solder is used instead of wire to provide the metallurgical means for forming interconnections. The advantages of using flip-chip interconection over conventional wire bonding include a greater number of available pins, smaller die size, shortened electrical connections, and increased manufacturing efficiency.

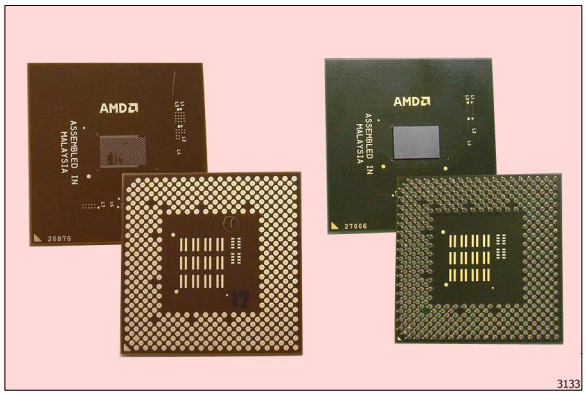

Figure 2.11 Samples of OPGA package, OGF 453.

AMD currently offers a 453 pin count in this package style (OGF 453). The table below provides an overview of this device. For details on the material content of each individual package, see *Chapter 4 Package Materials*.

Package Attributes: Organic Pin Grid Array

Package Code/Pin Count	OGF 453
Package Body Size (L x W) (nom, mm)	49.53 x 49.53
Pin Pitch (mm)	1.27
Package Body Thickness (to baseplane)[1] (nom, mm)	1.1[1]
Package Height[2] (max, mm)	6.41[2]
Coplanarity (mm)	N/A
Package Weight (grams)	Note[4]
Product Carrier[3]	Tray
JEDEC Moisture Sensitivity Rating	N/A
UL Flammability Rating and Oxygen Index	N/A

Notes:

1 Refers to substrate thickness only.
2 Includes standoff, substrate, chip, and pad.
3 See *Chapter 7 Trays* for further information.
4 Contact your AMD sales representative for this data.

Organic Micro Pin Grid Array. In order to meet customer demand for increased pin counts on smaller-sized packages, AMD has developed a new organic micro-PGA packaging design.

***Package Design*—**The pin arrangement on AMD's OµPGA package is more densely packed than that which is found on conventional OPGA packages, thus resulting in a smaller package size. AMD designs its OµPGA packages using flip chip interconnection.

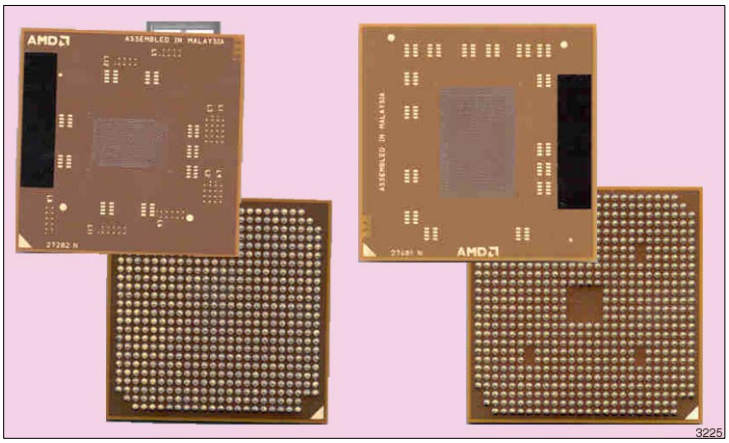

Figure 2.12 Samples of AMD's OµPGA packages.

AMD currently offers this package style in several pin counts. The table below provides an overview of each device. For details on the material content of each individual package, see *Chapter 4 Package Materials*.

Package Attributes: Organic Micro Pin Grid Array

Package Code/Pin Count	UOG 563	UOG 638	UOG 754
Package Body Size (L x W) (nom, mm)	33.00 x 33.0	35.00 x 35.00	40.00 x 40.00
Pin Pitch (mm)	1.27	1.27	1.27
Package Body Thickness[1] (to baseplane) (nom, mm)	0.14[1]	1.1[1]	1.17[1]
Package Height[2] (nom, mm)	2.7[2]	3.96[3]	6.53[4]
Coplanarity (mm)	N/A	N/A	N/A
Package Weight (grams)	Note[6]	Note[6]	Note[6]
Product Carrier[5]	Tray	Tray	Tray
JEDEC Moisture Sensitivity Rating	N/A	N/A	N/A
UL Flammability Rating and Oxygen Index	N/A	N/A	N/A

Notes:

1 Refers to substrate thickness only.
2 Includes standoff, substrate, chip, and pad.
3 Includes standoff, substrate, and chip.
4 Includes standoff, substrate, chip, and lid.
5 See *Chapter 7 Trays* for further information.
6 Contact your AMD sales representative for this data.